PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Tan et al.

Serial No.: 10/645,389

Filed: August 21, 2003

For: APPARATUS, SYSTEMS AND METHODS RELATING TO THE RECONSTRUCTION OF SEMICONDUCTOR WAFERS FOR WAFER-LEVEL PROCESSING AND RECONSTRUCTED SEMICONDUCTOR WAFERS

Confirmation No.: 8099

Examiner:

Group Art Unit: 2812

Attorney Docket No.: 2269-5528US

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 10, 2004
Date

ABlackburn
Signature

Aubry Blackburn
Name (Type/Print)

COMMUNICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed is a copy of Priority Document 200302784-4 filed May 7, 2003 for the above referenced application.

Respectfully submitted,

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Date: December 10, 2004
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Document in ProLaw

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This is to certify that the annexed is a true copy of following application as filed with the Registry.

Date of Filing	:	7 MAY 2003
Application Number	:	200302784-4
Applicant(s) / Proprietor(s) of Patent	:	MICRON TECHNOLOGY, INC.
Title of Invention	:	APPARATUS, SYSTEMS AND METHODS RELATING TO THE RECONSTRUCTION OF SEMICONDUCTOR WAFERS FOR WAFER-LEVEL PROCESSING AND RECONSTRUCTED SEMICONDUCTOR WAFERS

SHARMAINE WU (Ms)
Assistant Registrar
for REGISTRAR OF PATENTS
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5 OCTOBER 2004

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PRIORITY DOCUMENT

G00001

PATENTS FORM 1
Patents Act
(Cap. 221)
Patents Rules
Rule 19

INTELLECTUAL PROPERTY OFFICE OF SINGAPORE

REQUEST FOR THE GRANT OF A PATENT UNDER SECTION 25

101101

* denotes mandatory fields

1. YOUR REFERENCE* A3-0300 PYK/rsa

2. TITLE OF INVENTION* Apparatus, Systems and Methods relating to the Reconstruction of Semiconductor Wafers for Wafer-Level Processing and Reconstructed Semiconductor Wafers

3. DETAILS OF APPLICANT(S)* (see note 3) Number of applicant(s): 1

(A) Name: Micron Technology, Inc.

Address: 8000 South Federal Way
Boise

State: Idaho 83707-0006 Country: US

[X] For corporate applicant [ ] For individual applicant

State of incorporation: Delaware State of residency:

Country of incorporation: US Country of residency:

[ ] For others (please specify in the box provided below)

(B) Name:

Address:

State: Country:

ACTION

☐ For corporate applicant ☐ For individual applicant

State of incorporation | State of residency

Country of incorporation | Country of residency

☐ For others (please specify in the box provided below)

(C) Name

Address

State | Country

☐ For corporate applicant ☐ For individual applicant

State of incorporation | State of residency

Country of incorporation | Country of residency

☐ For others (please specify in the box provided below)

☐ Further applicants are to be indicated on continuation sheet 1

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4. DECLARATION OF PRIORITY (see note 5)

A. Country/country designated

File number | Filing Date DD MM YYYY

B. Country/country designated

File number | Filing Date DD MM YYYY

☐ Further details are to be indicated on continuation sheet 6

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5. INVENTOR(S)* (see note 6)

A. The applicant(s) is/are the sole/joint inventor(s) Yes ☐ No ☒

B. A statement on Patents Form 8 ~~is/will be~~ furnished Yes [X] No [ ]

6. CLAIMING AN EARLIER FILING DATE UNDER (see note 7)

[ ] section 20(3) [ ] section 26(6) [ ] section 47(4)

Patent application number

Filing Date (DD MM YYYY)

Please mark with a cross in the relevant checkbox provided below
(Note: Only one checkbox may be crossed.)

[ ] Proceedings under rule 27(1)(a)

Date on which the earlier application was amended (DD MM YYYY)

[ ] Proceedings under rule 27(1)(b)

7. SECTION 14(4)(C) REQUIREMENTS (see note 8)

Invention has been displayed at an international exhibition. Yes [ ] No [X]

8. SECTION 114 REQUIREMENTS (see note 9)

The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty.

Yes [ ] No [X]

9. CHECKLIST*

(A) The application consists of the following number of sheets

i	Request	5	Sheets
ii.	Description	13	Sheets
iii.	Claim(s)	10	Sheets
iv.	Drawing(s)	10	Sheets
v.	Abstract (Note: The figure of the drawing, if any, should accompany the abstract)	1	Sheets
Total number of sheets		39	Sheets

(B) The application as filed is accompanied by.

[ ] Priority document(s) [ ] Translation of priority document(s)

[X] Statement of inventorship & right to grant

[ ] International exhibition certificate

10. DETAILS OF AGENT (see notes 10, 11 and 12)

Name

Firm: Arthur Loke Bernard Rada & Lee

11. ADDRESS FOR SERVICE IN SINGAPORE* (see note 10)

Block/Hse No. | Level No. | Unit No./PO Box: 23-01

Street Name: 9 Temasek Boulevard

Building Name: Suntec Tower Two

Postal Code: 038989

12. NAME, SIGNATURE AND DECLARATION (WHERE APPROPRIATE) OF APPLICANT OR AGENT* (see note 12)
(Note: Please cross the box below where appropriate.)

[X] I, the undersigned, do hereby declare that I have been duly authorised to act as representative, for the purposes of this application, on behalf of the applicant(s) named in paragraph 3 herein.

Patsy Koh

Name and Signature

DD MM YYYY: 07/05/2003

NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the rest of the application. Please note that the filing fee should be furnished within the period prescribed.

2. The relevant checkboxes as indicated in bold should be marked with a cross where applicable.

3. Enter the name and address of each applicant in the spaces provided in paragraph 3.
   Where the applicant is an individual
   - Names of individuals should be indicated in full and the surname or family name should be underlined.
   -The address of each individual should also be furnished in the space provided.
   - The checkbox for "For individual applicant" should be marked with a cross.

   Where the applicant is a body corporate
   - Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided.
   - The address of the body corporate should also be furnished in the space provided.
   - The checkbox for "For corporate applicant" should be marked with a cross.

   Where the applicant is a partnership
   - The details of all partners must be provided. The name of each partner should be indicated in full and the surname or family name should be underlined.
   - The address of each partner should also be furnished in the space provided.
   - The checkbox for "For others" should be marked with a cross and the name and address of the partnership should be indicated in the box provided.

4. In the field for "Country", please refer to the standard list of country codes made available by the Registry of Patents and enter the country code corresponding to the country in question.

5. The declaration of priority in paragraph 4 should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under section 17 of the Patents Act] should be identified and the country should be entered in the space provided.

6. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph 5 should be completed by marking with a cross the 'YES' checkbox in the declaration (A) and the 'NO' checkbox in the alternative statement (B). Where this is not the case, the 'NO' checkbox in declaration (A) should be marked with a cross and a statement will be required to be filed on Patents Form 8.

7 When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified in paragraph 6 and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(a), they should also indicate the date on which the earlier application was amended.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' checkbox at paragraph 7 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' checkbox at paragraph 8 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross. Attention is also drawn to the Fourth Schedule of the Patents Rules.

10 Where an agent is appointed, the fields for "DETAILS OF AGENT" and "ADDRESS FOR SERVICE IN SINGAPORE" should be completed and they should be the same as those found in the corresponding Patents Form 41. In the event where no agent is appointed, the field for "ADDRESS FOR SERVICE IN SINGAPORE" should be completed, leaving the field for "DETAILS OF AGENT" blank.

11. In the event where an individual is appointed as an agent, the sub-field "Name" under "DETAILS OF AGENT" must be completed by entering the full name of the individual. The sub-field "Firm" may be left blank. In the event where a partnership/body corporate is appointed as an agent, the sub-field "Firm" under "DETAILS OF AGENT" must be completed by entering the name of the partnership/body corporate. The sub-field "Name" may be left blank.

12. Attention is drawn to sections 104 and 105 of the Patents Act, rules 90 and 105 of the Patents Rules, and the Patents (Patent Agents) Rules 2001.

13. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore In the latter case, no application should be made overseas until at least 2 months after the application has been filed in Singapore, and unless no directions had been issued under section 33 by the Registrar or such directions have been revoked. Attention is drawn to sections 33 and 34 of the Patents Act.

14. If the space provided in the patents form is not enough, the additional information should be entered in the relevant continuation sheet. Please note that the continuation sheets need not be filed with the Registry of Patents if they are not used.

APPARATUS, SYSTEMS AND METHODS RELATING TO THE RECONSTRUCTION OF SEMICONDUCTOR WAFERS FOR WAFER-LEVEL PROCESSING AND RECONSTRUCTED SEMICONDUCTOR WAFERS

TECHNICAL FIELD

The present invention relates to the processing of semiconductor wafers and dice. More particularly, but not necessarily limited thereto, it relates to reconstructing semiconductor wafers using only semiconductor dice that are not known to contain defects to retain the benefits of wafer-level processing while reducing resources spent on processing defective dice.

BACKGROUND

The advent of wafer-level processing has allowed for substantial savings and efficiency in the creation of microprocessors, as has been widely recognized throughout the industry. Unfortunately, however, almost all wafers contain some bad die sites where defective dice are created. Time and materials are thus wasted on fabricating defective dice.

Attempts have been made to reduce the amount of expensive materials or processing time that is wasted on die sites that are known to be defective on a wafer. One such approach is to track the defective dice on each wafer. As the wafer is processed, initial probe testing of the die sites is conducted as is appropriate. Die sites that are known to be defective are tracked by the processing equipment and, where possible, are omitted from subsequent processing steps. As the dice are singulated, the defective sites, although singulated, are not separated or "picked" from the wafer. While this approach allows for some savings, it cannot eliminate the use of certain resources on the defective die sites, such as equipment for wafer-level testing and burn-in, which is not susceptible, due to its configuration, for contacting only known good dice, or KGD. It would also require processing equipment that is configured and designed to track each die site on each wafer and then apply treatments and testing only to selected sites, which, in most instances, is not feasible. Other approaches involve singulation of the wafer at an early stage, followed by testing and treatment of dice individually, or attempts to repair defects on dice. Such approaches can be costly in

both the amount of handling, processing, and materials and in the additional processing time required.

A system or process that allows for the creation of a wafer that lacks any known defective die sites yet maintains the benefits of wafer-level processing would be advantageous. Such a process or method that could be used to form interconnect structures or add other functionality to a die would be further advantageous.

DISCLOSURE OF INVENTION

The present invention provides apparatus, systems and methods relating to the reconstruction of semiconductor wafers for wafer-level processing. Selected semiconductor dice having alignment cavities formed in a surface, such as the rear surface, thereof are placed in contact with alignment droplets of a material in a liquid, gel or other flowable state, which position the dice through surface tension interaction. Selected dice may be dice without known defects qualified during probe testing or dice recovered from damaged wafers. The alignment droplets may be disposed in a pattern corresponding to that of the alignment cavities on a reconstruction table, or on a fixture plate. The alignment droplets are solidified to maintain the die positioning and an underfill is disposed about the solidified alignment droplets to strengthen and maintain the reconstructed wafer. Where present, the fixture plate may add additional strength and simplify processing steps by providing structure for enhanced handling of the reconstructed wafer. The reconstructed wafer may undergo any desired wafer-level processing although the present invention is especially suitable for enhancing the utility of wafer-level testing and burn-in equipment used to qualify dice as "known good dice" or KGD. Where the alignment droplets are composed of sacrificial material, or the alignment cavities contain sacrificial material, this material may be removed from the reconstructed wafer. The resulting voids can be filled to form interconnects on the resulting dice. Where the voids are filled with conductive material, contact pads, connections or bumps may be formed.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings, which depict the best mode presently known for carrying out the invention:

FIG. 1 is a side view of one possible embodiment of a reconstruction table and fixture plate, useful with some embodiments in accordance with the present invention;

FIG. 2 is a side view of the reconstruction table and fixture plate of FIG. 1 with alignment droplets disposed thereon;

FIG. 3 is a side view of a reconstruction table in accordance with the present invention, with semiconductor dice disposed thereon, arranged in suitable positions by the alignment droplets;

FIG. 4 is a side view of the reconstruction table of FIG. 3, with an underfill disposed between the semiconductor dice and the fixture plate;

FIG. 5 is a side view showing one embodiment of a reconstructed wafer in accordance with the present invention separated from the reconstruction table;

FIG. 6 is a side view depicting the reconstructed wafer embodiment of FIG. 5 attached to an adhesive tape for back-grinding;

FIG. 7 is a side view depicting the reconstructed wafer of FIGS. 5 and 6 after a back-grinding process;

FIG. 8 is a side view of another embodiment of individual semiconductor dice singulated from the reconstructed wafer of FIG. 7;

FIG. 9 is a side view of some additional embodiments of semiconductor dice that are useful in some embodiments in accordance with the present invention;

FIG. 10 is a side view of a reconstruction table in accordance with the present invention, with the semiconductor dice of FIG. 9 disposed thereon, arranged in suitable positions by the alignment droplets;

FIG. 11 is a side view of the reconstruction table of FIG. 10, with an underfill disposed between the semiconductor dice and the reconstruction table;

FIG. 12 is a side view showing one embodiment of a reconstructed wafer in accordance with the present invention separated from the reconstruction table;

FIG. 12A is a top elevated view of a portion of the reconstructed wafer of FIG. 12;

FIG. 13 is a side view depicting the reconstructed wafer of FIG. 12 after a back-grinding process;

FIG. 14 is a side view of another embodiment of individual semiconductor dice singulated from the reconstructed wafer of FIG. 13;

FIG. 15 is a side view depicting the reconstructed wafer of FIG. 12 with a sacrificial material removed therefrom;

FIG. 16 is a side view depicting the reconstructed wafer of FIG. 15 with a selected replacement filler material filling the void created by the removal of the sacrificial material;

FIG. 17 is a side view depicting the reconstructed wafer embodiment of FIG. 16 attached to an adhesive tape for back-grinding; and

FIG. 18 is a side view depicting the reconstructed wafer of FIG. 17 with an underfill material removed therefrom.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

Turning to FIG. 1, there is depicted a reconstruction table 100. Reconstruction table 100 may be used as a platform for reconstructing a semiconductor wafer. One or more wafer reconstruction locations 101 may be present on the reconstruction table 100. In other words, a reconstruction table 100 may be configured for concurrent reconstruction of multiple wafers. A temperature control system 102, schematically represented by coils, may be present in connection with reconstruction table 100 and used to raise, lower, or maintain a desired temperature of the reconstruction table 100 and surrounding environment. In practice, temperature control system 102 may comprise resistive heating elements, passageways within reconstruction table 100 for circulating fluid of heating or cooling, semiconductor-type heat exchange modules, or other heat exchange systems known in the art. Further, one or more sensors 103 may be placed within (as shown) reconstruction table 100 or in contact therewith, sensors 103 being used with a controller 107 for modulating the temperature of reconstruction table 100 in each region or portions thereof.

At each reconstruction location 101, a plurality of patterns of alignment vias 104 open out at the surface of a substrate comprising reconstruction table 100, each in communication with an alignment material delivery system 105. A fixture plate 110 may be disposed on the reconstruction table 100. Fixture plate 110 has a plurality of patterns of vias 106 that align with the alignment vias 104 when placed on a reconstruction location 101 on reconstruction table 100. Fixture plate 110 may be formed of any suitable material, including polymeric materials, crystalline silicon, glass,

steel, aluminum or any other suitable material known to those of ordinary skill in the art and desirable for the processing involved. For example, where subsequent processing steps require the rear surface of a wafer to be silicon, a silicon fixture plate 110 may be selected. Alternate embodiments of the process may occur without the use of a fixture plate 110. For example, a resulting wafer lacking a fixture plate 110 may be removed from the reconstruction table 100 following underfill (which will be discussed below). To facilitate such a procedure, the reconstruction location 101 may be coated with a compound to aid in the release of a completed wafer therefrom.

As shown in FIG. 2, using an alignment material delivery system 105, an alignment material 108 is delivered in a liquid, gel or other flowable state through at least one alignment via 104 (and corresponding via 106 of fixture plate 110 where present) to form at least one alignment droplet 112 at the reconstruction location 101, atop the fixture plate 110 where present. Desirably, a number of alignment droplets 112 will be formed into a desired pattern by the arrangement of a number of alignment vias 104, as will be explained in more detail further herein.

Turning to FIG. 3, a plurality of semiconductor dice 120 are shown disposed at the reconstruction location 101. Dice 120 may be selected by qualification using wafer probe testing, visual inspection of dice sites on a wafer, or as otherwise desired and known to those of ordinary skill in the art. Each die 120 may be formed of silicon, gallium arsenide, indium phosphide or other suitable semiconductor material and includes at least one alignment cavity 122 and preferably a pattern thereof, located on a rear surface 123 thereof. For purposes of facilitating the understanding of the invention, the die 120 will be referred to as having an active surface 121 as the "front" of the die with an opposite rear surface 123. It will be understood that such terms are for making relative positions clear and do not limit the invention. Alignment cavities 122 may be formed in the rear surface 123 of each die 120 using any suitable method for forming vias, cavities, or trenches in semiconductor substrates known to those of ordinary skill in the art. For example, the alignment cavities 122 may be formed by wet etching, dry etching (and comprise either isotropic etching or anisotropic etching), laser ablation, drilling or boring with a mechanical drill bit, or otherwise as known to those of ordinary skill in the art. Although embodiments utilizing a single alignment cavity 122 may be designed and are within the scope the present invention, it is currently preferred to use a

plurality of patterns of alignment cavities 122 on the rear surface 123, in order to allow the die 120 to be correctly positioned in multiple directions, being the X and Y directions parallel to the plane of reconstruction table 100 as well as rotationally in the same plane. For example, one or more parallel rows of alignment cavities 122 or a pattern of alignment cavities 122 (for example, patterns of four cavities in each die 120 to be aligned) may be formed on the rear surface of each die. It will be appreciated that any desirable or advantageous arrangement of the alignment cavities 122 on the rear (non-active) surface of the die 120 may be used and all such patterns and arrangements are within the scope of the present invention.

Each alignment cavity 122 may be formed to any desired depth in the die 120, so long as it is sufficient to enable the alignment of the die 120 when interacting with a corresponding alignment droplet 112, as will be explained further herein. For some embodiments, one or more alignment cavities 122 may be used as vias connecting the active surface 121 of the die 120 to the rear surface 123, increasing throughput by using a single structure for multiple purposes, and enabling novel methods of forming die 120 interconnects or bumped dice for flip-chip applications. Such embodiments will be discussed in more detail further herein.

As a die 120 is placed into the reconstruction location 101 by, for example, conventional and suitably programmed pick and place equipment, it is roughly aligned with a desired final position in the resulting reconstructed wafer. The alignment droplet(s) 112 thus make contact with one or more alignment cavities 122 on the rear surface 123 of the die 120. The die 120 is then released and surface tension of the alignment droplets 112 interacts with the similarly patterned alignment cavities 122 to position the die 120 in its final, precise alignment and hold the die 120 in the correct, desired position. By positioning patterns of droplets 112 in the reconstruction location 101 to define locations of dice 120 for reconstruction of a wafer, a plurality of dice 120 may be aligned in proper positions with respect to one another to form a reconstructed wafer for further wafer-level processing. Achieving and maintaining proper positioning among the dice is important and required to allow processing of the reconstructed wafer to take place with conventional equipment.

Once a desired number of dice 120 are correctly aligned in the proper positions, the alignment droplets 112 are then at least partially solidified to retain the dice 120 in

the correct positions. For example, using the temperature control system 102, the temperature of the reconstruction table 100 may be raised or lowered to effect an at least partial solidification of a liquid alignment material 108 comprising alignment droplets 112, solidifying the liquid alignment material 108 and adhering the solidified alignment droplets 112 to the dice 120. For example, using a thermoplastic resin as the alignment material 108, the thermoplastic resin may be heated to melt and delivered to form alignment droplets 112, following which the temperature may be cooled or allowed to cool to a point where the alignment material 108 at least partially solidifies. As another example, a thermoset resin may be used as the alignment material 108, pumped through the alignment vias 104 to form alignment droplets 112 and then heated using temperature control system 102 to solidify. A third exemplary alignment material 108 may be a liquid epoxy that is heat cured to solidify. With such embodiments, where necessary, the temperature of the alignment vias 104 may be separately maintained at a lower level to prevent solidification therein. An additional example of a suitable alignment material may be a low melting point metal, such as a tin/lead solder, silver solder or other low melting point metals or alloys. The low melting point metal may be melted and delivered to form alignment droplets 112 and then cooled, or allowed to cool, to solidify. It will, of course, be appreciated that alternative processes for solidifying alignment droplets 112 may be used and are within the scope of the present invention, such as the application of a chemical setting agent, the exposure of alignment droplets 112 of a photoreactive alignment material 108 to an appropriate wavelength of light, such as a photopolymer curable using exposure to radiation (as, for example, polymers that are liquid when heated and gel upon exposure to radiation, such as UV light, x-rays, microwaves, etc.), or any other process known to those of ordinary skill in the art.

Once alignment droplets 112 are at least partially solidified, an underfill material 126, such as an epoxy, may be disposed under the dice 120. The embodiment of FIG 3, with an underfill material 126 disposed between the dice 120 and the fixture plate 110, is shown in FIG. 4. Various dielectric underfill materials 126, such as conventional underfill epoxies, are known to those of ordinary skill in the art and any suitable underfill material may be employed to retain the die 120 to the fixture plate 110 or otherwise solidify the positions of dice 120 in the reconstructed wafer. Once the

underfill material 126 has cured, a reconstructed wafer 130 is formed and may be removed with fixture plate 110 (if used) from the reconstruction table 100, as shown in FIG. 5. The reconstructed wafer 130 then may undergo any desired wafer-level processing to complete the fabrication of the dice 120 or for creation of complete multidie semiconductor assemblies. For example, the reconstructed wafer 130 may undergo wafer-level testing and burn-in to qualify dice 120 thereof as KGD, although it will be appreciated that any desired wafer-level treatment such as wafer-level rerouting or wafer-level treatments for packaging may be performed on the reconstructed wafer 130.

It will be appreciated that the term "reconstructed wafer," as used herein, means any reconstructed bulk substrate including semiconductor dice. Such reconstructed wafers may have any desired shape, including a conventional round wafer shape, which may be desirable for processing with conventional wafer handling and processing equipment. Other embodiments may produce square or rectangular reconstructed wafers, which may be desirable for use with testing equipment. All such shapes are within the scope of the present invention.

Once wafer-level processing is complete, the reconstructed wafer 130 may then be singulated into a number of separate dice 120, which may be KGD, as previously noted. One process for singulation is depicted in FIGS. 6, 7 and 8. The reconstructed wafer 130 is attached to a film of adhesive-coated polymer 132, as in a conventional wafer back-grinding process, with the active surface 121 of the dice 120 adhered to the film 132, as depicted in FIG. 6. The reconstructed wafer 130 is then back-ground, removing the fixture plate 110 (where present), the underfill material 126 and the alignment drops 112. Where the dice 120 are of sufficient depth or thickness, the back-grinding may continue to remove the alignment cavities 122 and the remainder of alignment droplets 112 located therein and any desired portion of the wafer thickness, resulting in the structure shown in FIG. 7 of a number of thinned dice 120 attached to the film 132. The individual finished dice 120 may then be separated by simply removing the film 132, as depicted in FIG. 8. Of course, it will be appreciated that any alternative method for wafer singulation known to those of ordinary skill in the art may be used to separate the dice 120. For example, the reconstructed wafer may be singulated with a conventional wafer saw or by any other suitable technique.

The foregoing method thus enables creation of a reconstructed wafer using only dice 120 that have no visible defects, or dice 120 that through probe testing have been determined to be at least functional. Additional changes and refinements may be made to the basic method and all such refinements are within the scope of the present invention.

Some embodiments of processes in accordance with the present invention may be used to form interconnects or other structures as a reconstructed wafer is formed or dice 120 are singulated therefrom. Examples of such processes are depicted in FIGS. 9 through 18 as discussed below.

FIG. 9 depicts several different dice 220A, 220B and 220C that may be used in practicing certain embodiments of the present invention. Different alignment via 222 treatments have been applied to each die 220A, 220B and 220C. The alignment vias 222 of die 220A comprise at least one via 222A that passes through the thickness of the entire die, allowing contact between the active surface 221 and the rear surface 223 therethough. Where desirable, a suitable coating may be placed on the interior surface of the via 222A. For example, an insulative coating may be placed on the via 222A walls to protect the die 220A from the inductive effects of a current passing through conductive material later filling the via 222A. Alternatively, a conductive coating may be applied to form part of a conductive interconnection structure.

The alignment vias 222 of die 220B similarly comprise at least one via 222B that passes through the thickness of the die 220B. Via 222B is partially filled with a selected filler material 225, such as a sacrificial material or a conductive material that can be in electrical communication with the integrated circuit formed on the active surface 221 of the die 220B. Desirably, via 222B is filled from 1/4 to 3/4 with the selected filler material 225, although any other partial filling may be used. Similarly, the at least one alignment via 222C of die 220C passes through the thickness of the die 220C, but is filled with selected filler material 225 substantially throughout its depth. It will, of course, be appreciated that the walls of alignment holes 222B and 222C may be coated with any desired coatings prior to filling with the selected filler material 225.

As shown in FIG. 10, a number of alignment droplets 112 are extruded through the reconstruction table 100, and the dice 220A, 220B, 220C are disposed thereon, such that the interaction of the surface tension of the alignment droplets 112 aligns dice 220A, 220B, 220C for exact placement in a reconstructed wafer, as has been discussed previously herein. It will be appreciated that the alignment droplet 112 size may be controlled to result in filling the volume of the alignment vias 222A-222C that has not been filled previously with a selected filler material with the alignment droplet 112. In the case of an "empty" via, such as 222A, this can result in a via filled with the alignment material 108 or a via partially filled with alignment material 108. For a partially empty via, such as 222B, this results in a via partially filled with selected filler material 225 with the remainder filled by alignment material 108. In the case of a filled alignment via 222C, the material of the alignment material 108 is selected to "wet" to the filler material 225, so that the surface tension of alignment droplets 112 is effective to align die 220C. Where desired, the alignment material 108 may be a conductive material, such as a metallic solder, a conductive polymer, or a polymer containing conductive material suspended therein. Alternatively, the alignment material 108 may comprise a sacrificial material. It will be appreciated that the term "sacrificial material" as used herein refers to any material, or compound, that may be utilized for a specific function in any process or method of the present invention and then be removed at a later stage of such process or method. For example, where the alignment droplets 112 are back-ground from the die 120, as discussed previously herein, such alignment droplets 112 are considered to be a sacrificial material. Sacrificial materials may be selected to facilitate their removal after use, as will be discussed further herein.

The alignment droplets 112 are then heated, cooled, or otherwise treated to at least partially solidify and an underfill material 126 is disposed underneath the dice 220A, 220B, 220C and around the solidified alignment droplets 112, resulting in the structure seen in FIG. 11. Once the underfill 126 has set or otherwise solidified, the reconstructed wafer 230 may then be removed for processing as discussed previously herein and depicted in FIG. 12. An elevated view of a portion of the reconstructed wafer 230 is shown in FIG. 12A.

At this point, the reconstructed wafer 230 may undergo any wafer-level processing that is desired as is discussed previously herein. Wafer-level burn-in and testing may even be conducted. Where the alignment material 108 selected is a conductive material and, if present, the selected filler material 225 is also conductive and makes contact with the patterns of the active surface of the die 220a, 220B, 220C, testing and burn-in may be effected by making electrically communicative contact with the solidified alignment material 108 as exposed at the rear surface of the reconstructed wafer 230, as through the vias 106 of a fixture plate 110.

Following the wafer-level processing, the reconstructed wafer 230 may then be singulated into a number of separate dice 220A, 220B, 220C. Similar to that discussed previously herein, one process for doing so is depicted in FIGS. 13 and 14. The reconstructed wafer 230 is attached to a length of adhesive-coated film 132, as in a conventional wafer back-grinding process, with the active surfaces 221 of the dice 220A, 220B, 220C adhered to the film 132. The reconstructed wafer 230 is then back-ground, removing the fixture plate 110 (where present), the underfill material 126 and the alignment material 108 or selected filler material 225 that is present in the portion of the dice 220A, 220B, 220C that are back-ground. This results in a number of thinned dice 220A, 220B, 220C attached to the film 132, similar to that depicted in FIG. 7. Each finished die 220A, 220B, 220C contains a via 222A, 222B, 222C across the width thereof that is filled either with the selected filler material 225 or the alignment material 108. Where the alignment material 108 alone or in combination with a contacting selected filler material 225 is conductive and is in electrical communication with the active surface 221 of the dice 220A, 220B, 220C, this provides contacts 226 on the rear surfaces 223 of the dice that may be utilized in mounting the dice 220A, 220B, 220C in a complete semiconductor package or in an appropriate device. Individual finished dice 220A, 220B, 220C may be separated by simply removing the film 132, as depicted in FIG. 14. Of course, it will be appreciated that any alternative method for wafer singulation known to those of ordinary skill in the art may be used to separate the dice 220A, 220B, 220C.

Some additional processing embodiments, in accordance with the principles of the present invention, are depicted in FIGS. 15 through 18. A reconstructed wafer 230A is created as discussed previously herein in connection with FIGS. 9 through 12. At this

point, the reconstructed wafer may undergo any desired wafer-level processing procedure. Then, if a fixture plate 110 was used in creating the wafer, the fixture plate 110 is removed, mechanically by back-grinding or by forming the fixture plate 110 from a material that may be dissolved or by removing the fixture plate 110 with treatment by a suitable release agent. Of course, the need for this procedure may be eliminated by creating the reconstructed wafer 230A that lacks a fixture plate 110.

The alignment droplets 112 are thus at least accessible, if not partially exposed, through the underfill material 126 which holds the reconstructed wafer 230A together. Where the alignment material 108 is comprised of a sacrificial material, the alignment material 108 may then be removed from the reconstructed wafer 230A. Where the selected filler material 225 is a sacrificial material, it may also be removed. Removal of the sacrificial material may be accomplished in any manner suitable for the specific sacrificial material at issue. For example, a selective chemical etch may be performed to remove the sacrificial material. Alternatively, where appropriate, the temperature of the reconstructed wafer 230A may be lowered or raised to reverse the alignment material 108 phase change and allow a sacrificial material that is no longer solid to be removed by application of a vacuum or by a flushing or draining procedure.

Once the sacrificial material is removed, the reconstructed wafer 230A contains at least one void 240 in the underfill material 126 that corresponds to a removed alignment droplet 112 and may be connected to an at least partially empty alignment via, such as those depicted as 222A and 222B in FIG. 15. At this point, the vacated volume may be filled with a selected replacement filler material 242, as is desired. For example, the selected replacement filler material 242 may be a conductive metal or alloy, such as tin/lead solder, gold or a conductive polymer or conductively filled polymer to create a conductive structure through the via 222A, 222B, 222C and an integral conductive bump 244 on the rear surface 223, as depicted in FIG. 16. Of course, it will be appreciated that any desired selected replacement filler material 242 may be used.

The reconstructed wafer 230A may then undergo any additional desired wafer-level processing. It may be advantageous to attach the active surface of the reconstructed wafer 230A to a length of adhesive-coated film 132 to protect the active surfaces 221 of the dice 220A, 220B, 220C, as depicted in FIG. 17. This procedure may

occur during processing, or prior to removal of the sacrificial material. Processing of the wafer at this stage may include wafer testing and burn-in of the dice 220A, 220B, 220C using conductive bumps 244 as contacts.

The underfill material 126 may then be removed from the reconstructed wafer to substantially fully expose the conductive bumps 244. This may be accomplished in any suitable manner, such as by selectively removing the underfill material 126 through a chemical etch process, or by selecting an underfill material that can be induced to reflow from the reconstructed wafer under appropriate conditions. Removal of the underfill material results in dice 220A, 220B, 220C with substantially fully exposed bumps 244 similar to those depicted in FIG. 18. Of course, it will be appreciated that some embodiments in which the underfill material is not removed may be utilized and are within the scope of the present invention.

The individual dice 220A, 220B, 220C may be singulated from the reconstructed wafer 230A. Where the underfill material 126 has been removed, similar to the embodiment depicted in FIG. 18, this may be accomplished by removing the dice 220A, 220B, 220C from the adhesive-coated film 132, as has been discussed previously herein. Alternatively, singulation of the reconstructed wafer 230 may be accomplished using wafer sawing techniques. Where adhesive-coated film 132 has been applied to the active surface of the reconstructed wafer 230A, this leaves a protective layer on the active surfaces 221 of the resulting dice 220A, 220B, 220C. Alternatively, singulation may not be effected and the dice 220A, 220B, 220C may be marketed or used as multidie assemblies. Of course, an adhesive-coated film 132 that is susceptible to chemical etching or other non-mechanical severance or removal may be used and such singulation is also within the scope of the present invention.

Using the processes, equipment and methods in accordance with the present invention, reconstructed wafers 230 can be created that include only known good dice. These reconstructed wafers may then be processed in the same manner as any other wafer, using standard wafer-level processing equipment.

It will be apparent that details of the apparatus and methods herein described can be varied considerably without departing from the concept and scope of the invention. The claims alone define the scope of the invention as conceived and as described herein.

CLAIMS

What is claimed is:

1. A process for reconstructing a semiconductor wafer, comprising:

forming at least a first alignment droplet and at least a second alignment droplet from a flowable alignment material at laterally spaced locations on a substrate;

placing a first semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by surface tension thereof;

placing a second semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the second semiconductor die makes contact with the at least a second alignment droplet and is positioned by surface tension thereof;

inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify to maintain positions of the first semiconductor die and the second semiconductor die; and

introducing an underfill material adjacent the surfaces of the first and second semiconductor dice and surrounding the at least a first alignment droplet and the at least a second alignment droplet to form a reconstructed semiconductor wafer.

2. The process according to claim 1, wherein forming at least a first alignment droplet and at least a second alignment droplet from a flowable alignment material comprises extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form the at least a first alignment droplet and the at least a second alignment droplet.

3. The process according to claim 2, wherein extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form at least a first alignment droplet and at least a second alignment droplet comprises extruding the alignment material from a supply of alignment material operably coupled to a reconstruction table.

4. The process according to claim 2, wherein the substrate comprises a fixture plate and wherein extruding the flowable alignment material through at least a first alignment via and at least a second alignment via to form at least a first alignment droplet and at least a second alignment droplet comprises extruding the flowable alignment material through alignment vias located in the fixture plate to form part of the reconstructed semiconductor wafer.

5. The process according to claim 1, wherein inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die comprises at least one of raising or lowering a temperature of the alignment material to at least partially solidify the alignment droplets.

6. The process according to claim 1, wherein inducing the at least a first alignment droplet and the at least a second alignment droplet to at least partially solidify and maintain the positions of the first semiconductor die and the second semiconductor die comprises reacting the alignment material with an activating agent to at least partially solidify the alignment droplets.

7. The process according to claim 1, wherein placing a first semiconductor die having at least one alignment cavity on a surface thereof, such that the at least one alignment cavity of the first semiconductor die makes contact with the at least a first alignment droplet and is positioned by the surface tension thereof comprises placing a semiconductor die having a plurality of alignment cavities on a surface thereof, each of the alignment cavities interacting with a correspondingly positioned alignment droplet to position the semiconductor die.

8. The process according to claim 7, wherein placing a semiconductor die having a plurality of alignment cavities on a surface thereof comprises placing a semiconductor die having a grid pattern of alignment cavities.

9. The process according to claim 1, wherein introducing an underfill material adjacent the surfaces of the first and second semiconductor dice and surrounding the at least a first alignment droplet and the at least a second alignment droplet comprises introducing the underfill material between the first and second semiconductor dice and the substrate in the form of a fixture plate.

10. The process according to claim 1, further comprising curing the underfill material to a substantially solid state.

11. The process according to claim 1, further comprising singulating the first semiconductor die and the second semiconductor die from the reconstructed semiconductor wafer.

12. The process according to claim 11, wherein singulating the first semiconductor die and the second semiconductor die from the reconstructed semiconductor wafer comprises back-grinding the reconstructed semiconductor wafer to remove the underfill material.

13. The process according to claim 12, wherein back-grinding the reconstructed semiconductor wafer to remove the underfill material further comprises removing a fixture plate adhered to the underfill material by back-grinding the reconstructed semiconductor wafer.

14. The process according to claim 12, further comprising adhering active surfaces of the first semiconductor die and the second semiconductor die to an adhesive-coated film before singulating.

15. The process according to claim 14, further comprising removing the adhesive-coated film following the back-grinding.

16. A process for forming interconnective structures on a semiconductor die, the process comprising:

forming at least a first alignment droplet from a flowable alignment material;

placing a semiconductor die having at least one alignment cavity on a rear surface thereof, such that the at least one alignment cavity makes contact with the at least a first alignment droplet and is positioned by surface tension thereof;

inducing the at least a first alignment droplet to at least partially solidify and maintain a position of the semiconductor die;

introducing an underfill material adjacent the rear surface of the semiconductor die and surrounding the at least a first alignment droplet;

removing the alignment material from the surrounding underfill material to create at least one interconnect void adjacent the at least one alignment cavity;

filling the at least one interconnect void with an interconnect material to form at least one interconnect structure.

17. The process according to claim 16, further comprising removing the underfill material to substantially expose the at least one interconnect structure.

18. The process according to claim 16, wherein the at least one alignment cavity passes through an entire depth of the semiconductor die.

19. The process according to claim 18, wherein placing a semiconductor die having at least one alignment cavity on a rear surface thereof comprises placing a semiconductor die having at least one alignment cavity that substantially extends to an active surface of the semiconductor die.

20. The process according to claim 19, wherein placing a semiconductor die having at least one alignment cavity that substantially extends to an active surface of the semiconductor die comprises placing a semiconductor die where at least one alignment cavity is at least partially filled with a filler material.

21. The process according to claim 20, wherein placing a semiconductor die where at least one alignment cavity is at least partially filled with a filler material comprises placing a semiconductor die where at least one alignment cavity is at least partially filled with an electrically conductive filler material.

22. The process according to claim 21, further comprising removing the filler material from the at least one alignment cavity as the alignment material is removed from the surrounding underfill material to form an interconnect void including the at least one alignment cavity.

23. The process according to claim 16, wherein filling the at least one interconnect void with an interconnect material to form at least one interconnect structure comprises filling the at least one interconnect void with a conductive interconnect material to form at least one conductive interconnect structure.

24. The process according to claim 16, wherein forming at least a first alignment droplet from a flowable alignment material comprises extruding the flowable alignment material through at least a first alignment via to form the at least a first alignment droplet.

25. The process according to claim 24, wherein extruding the flowable alignment material through at least a first alignment via to form at least a first alignment droplet comprises extruding the flowable alignment material through an alignment via located in a reconstruction table.

26. The process according to claim 24, wherein extruding the flowable alignment material through at least a first alignment via to form at least a first alignment droplet comprises extruding the flowable alignment material through an alignment via located in a fixture plate.

27. The process according to claim 16, wherein inducing the at least a first alignment droplet to at least partially solidify and maintain the position of the semiconductor die comprises at least one of raising or lowering a temperature of the alignment material to at least partially solidify the at least a first alignment droplet.

28. The process according to claim 16, wherein inducing the at least a first alignment droplet to at least partially solidify and maintain the position of the semiconductor die comprises reacting the alignment material with an activating agent to at least partially solidify the at least a first alignment droplet.

29. The process according to claim 16, wherein placing a semiconductor die having at least one alignment cavity on a rear surface thereof, such that the at least one alignment cavity of the semiconductor die makes contact with the at least a first alignment droplet and is positioned by the surface tension thereof comprises placing a semiconductor die having a plurality of alignment cavities on the rear surface thereof, each of the alignment cavities of the plurality interacting with a correspondingly positioned alignment droplet to position the semiconductor die.

30. The process according to claim 16, wherein forming at least a first alignment droplet from a flowable alignment material comprises extruding the flowable alignment material through a substrate comprising a fixture plate and introducing an underfill material adjacent the rear surface of the semiconductor die and surrounding the at least a first alignment droplet comprises introducing the underfill material between the semiconductor die and the fixture plate.

31. The process according to claim 30, further comprising curing the underfill material to a substantially solid state.

32. A reconstructed semiconductor wafer comprising:

a plurality of semiconductor dice, each semiconductor die having at least a first alignment via disposed in a rear surface thereof;

a plurality of alignment droplets disposed adjacent the rear surfaces of the plurality of semiconductor dice, each of the at least a first alignment via in contact with a solidified alignment droplet; and

an underfill material disposed adjacent the rear surfaces of the plurality of semiconductor dice and around the alignment droplets.

33. The reconstructed semiconductor wafer of claim 32, further comprising a fixture plate adjacent the plurality of alignment droplets, such that the underfill material is disposed between the rear surfaces of the semiconductor dice and the fixture plate.

34. The reconstructed semiconductor wafer of claim 32, wherein the at least a first alignment via extends from the rear surface of each semiconductor die to an active surface thereof.

35. The reconstructed wafer of claim 34, wherein the at least a first alignment via is filled with a material comprising the alignment droplets.

36. The reconstructed wafer of claim 34, wherein the at least a first alignment via is at least partially filled by a selected filler material.

37. The reconstructed wafer of claim 32, wherein the plurality of alignment droplets comprises a conductive material.

38. A method of performing wafer-level processing on a number of separate semiconductor dice, the method comprising:

selecting a plurality of semiconductor dice;

forming at least one alignment via on a rear surface of each semiconductor die of the plurality;

positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets positioned on a substrate and using surface tension of the alignment droplets to effect precise alignment of the semiconductor dice;

underfilling the positioned semiconductor dice to form a reconstructed semiconductor wafer; and

performing wafer-level processing on the reconstructed semiconductor wafer.

39. The method of claim 38, wherein selecting a plurality of semiconductor dice comprises selecting a number of known functional dice.

40. The method of claim 38, wherein positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets further comprises inducing the alignment droplets to at least partially solidify to maintain the proper positions.

41. The method of claim 40, wherein inducing the alignment droplets to at least partially solidify to maintain the proper positions comprises at least one of raising or lowering a temperature of the alignment droplets.

42. The method of claim 38, wherein the substrate comprises a fixture plate and wherein positioning the semiconductor dice in proper positions to form a semiconductor wafer by placing the at least one alignment via in contact with corresponding alignment droplets comprises placing the at least one alignment via in contact with corresponding alignment droplets disposed on the fixture plate.

43. The method of claim 42, wherein underfilling the positioned semiconductor dice to form a reconstructed semiconductor wafer comprises introducing an underfill material between the rear surfaces of the semiconductor dice and a surface of the fixture plate.

44. The method of claim 38, wherein performing wafer-level processing on the reconstructed semiconductor wafer comprises performing a wafer-level testing operation on the reconstructed semiconductor wafer.

45. The method of claim 38, wherein performing wafer-level processing on the reconstructed semiconductor wafer comprises performing burn-in at the wafer level on the reconstructed semiconductor wafer.

46. A reconstruction table comprising:

a platform comprising at least one reconstruction location where at least a first alignment via opens out at a surface of the platform;

a temperature control system for maintaining a desired temperature; and

an alignment material delivery system in communication with the at least a first alignment via, whereby an alignment material may be delivered in a flowable state through the at least a first alignment via to form at least one alignment droplet at the at least one reconstruction location.

47. The reconstruction table of claim 46, wherein the temperature control system includes a temperature-modifying structure selected from the group comprising a resistive heating element, a passageway for circulating fluid within the reconstruction table, and a semiconductor-type heat exchange module.

48. The reconstruction table of claim 46, wherein the temperature control system comprises at least one sensor for monitoring a temperature of the reconstruction table.

49. The reconstruction table of claim 48, wherein the temperature control system further comprises a controller for modulating the temperature of the reconstruction table in response to monitoring by the at least one sensor.

50. The reconstruction table of claim 46, wherein the at least one reconstruction location where at least a first alignment via opens out at the surface of the platform comprises a plurality of alignment vias that open out at the at least one reconstruction location, each of the plurality in communication with the alignment material delivery system.

51. The reconstruction table of claim 46, wherein the platform comprising at least one reconstruction location where at least a first alignment via opens out at the surface of the platform comprises a platform including a plurality of reconstruction locations where at least a first alignment via opens out at the surface of the platform.

APPARATUS, SYSTEMS AND METHODS RELATING TO THE RECONSTRUCTION OF SEMICONDUCTOR WAFERS FOR WAFER-LEVEL PROCESSING AND RECONSTRUCTED SEMICONDUCTOR WAFERS

ABSTRACT OF THE DISCLOSURE

Apparatus, systems and methods relating to the reconstruction of semiconductor wafers for wafer-level processing. Selected semiconductor dice having alignment cavities formed in a surface thereof are placed in contact with liquid, gel or other flowable alignment droplets in a similar pattern protruding from a substrate to position the dice through surface tension interaction. The alignment droplets are then solidified to maintain the positioning and an underfill is disposed between the dice and the fixture to strengthen and maintain the reconstructed wafer. A fixture plate may be used in combination with the underfill to add additional strength and simplify handling. The reconstructed wafer may be subjected to wafer-level processing, wafer-level testing and burn-in being particularly facilitated using the reconstructed wafer. Alignment droplets composed of sacrificial material may be removed from the reconstructed wafer and the resulting void filled to form interconnects or contacts on the resulting dice.

[Figure 12]

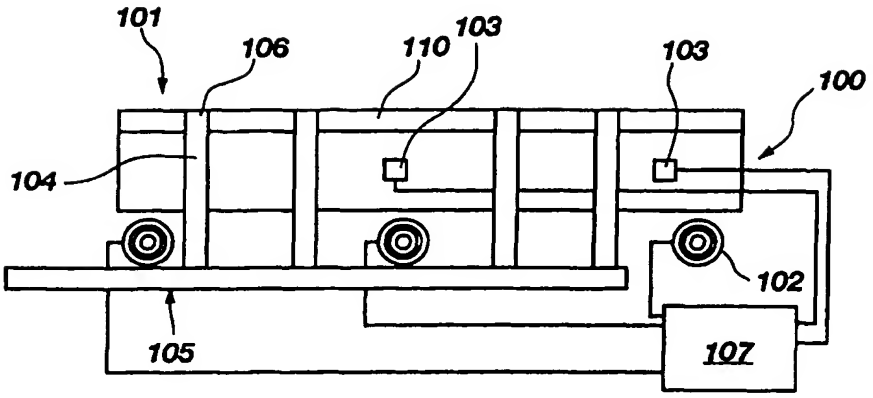


FIG. 1

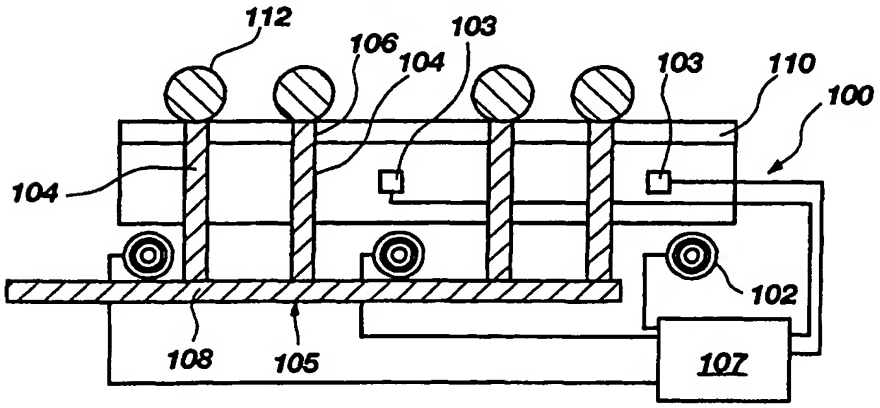
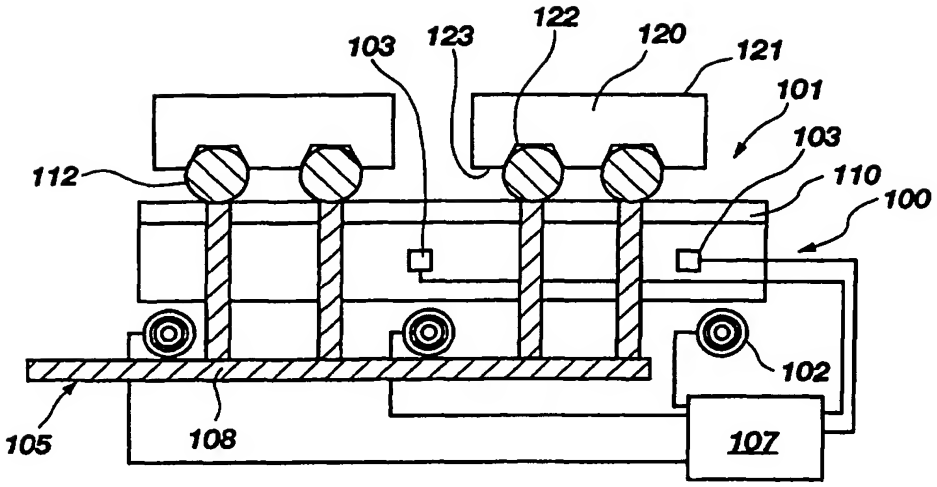


FIG. 2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123
122
120
121
101
103
110
100
112
102
105
108
107

FIG. 3

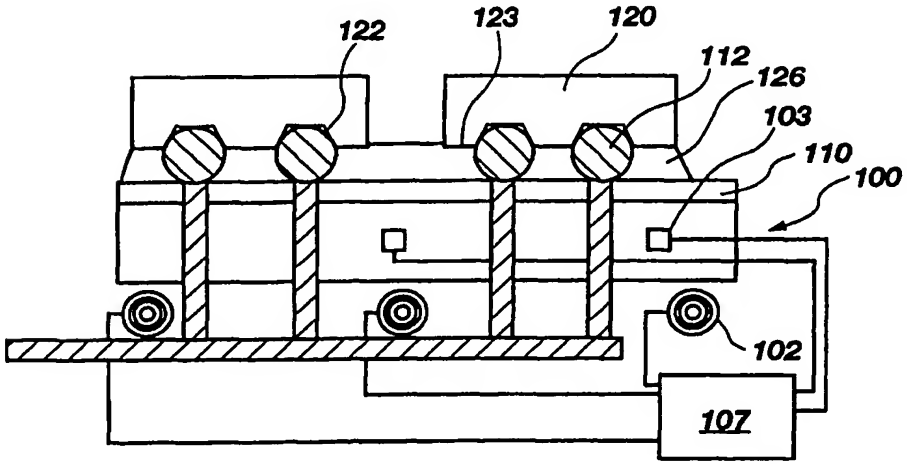

122
123
120
112
126
103
110
100
102
107

FIG. 4

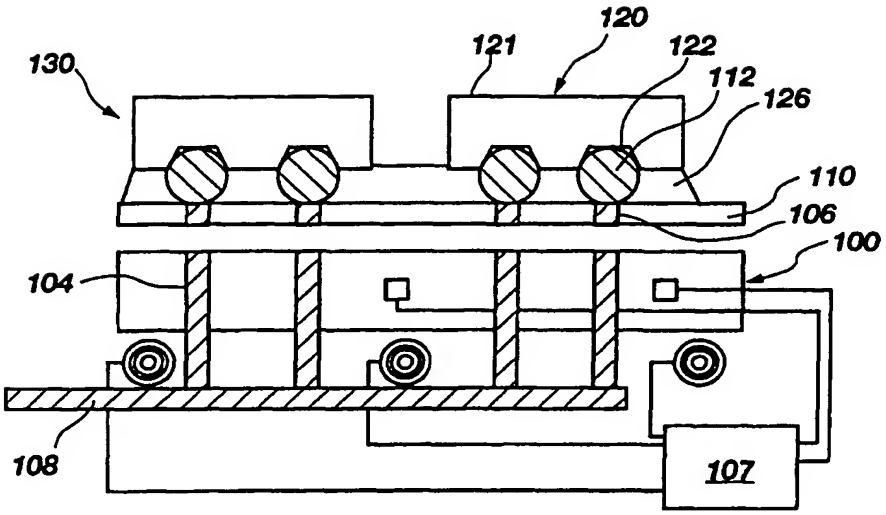


FIG. 5

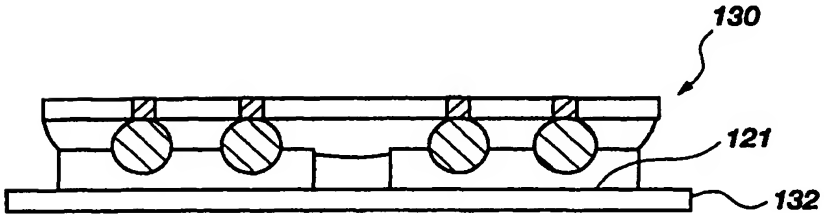


FIG. 6

FIG. 7

FIG. 8

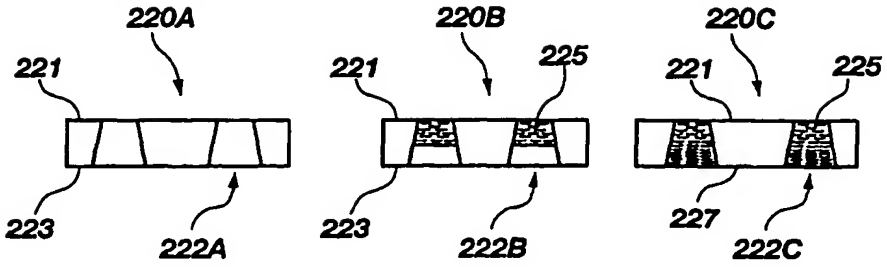

220A
221
223
222A
220B
221
225
223
222B
220C
221
225
227
222C

FIG. 9

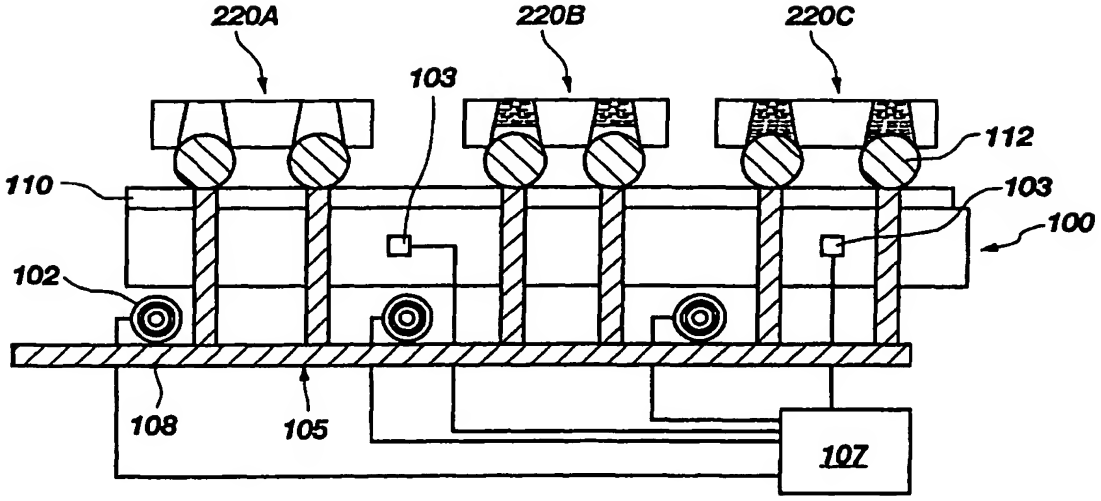

220A
220B
220C
103
112
110
103
100
102
108
105
10Z

FIG. 10

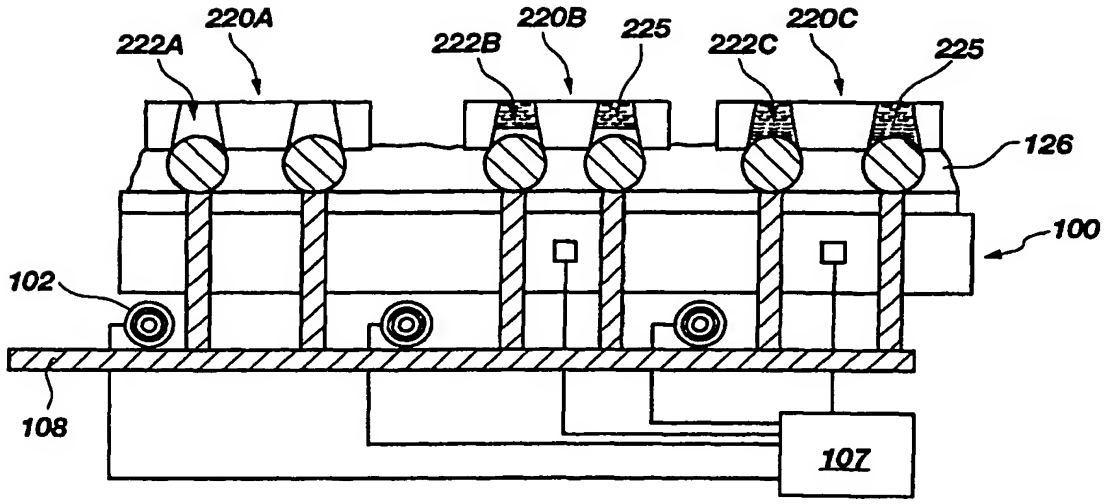

220A
222A
220B
222B
225
220C
222C
225
126
100
102
108
107

FIG. 11

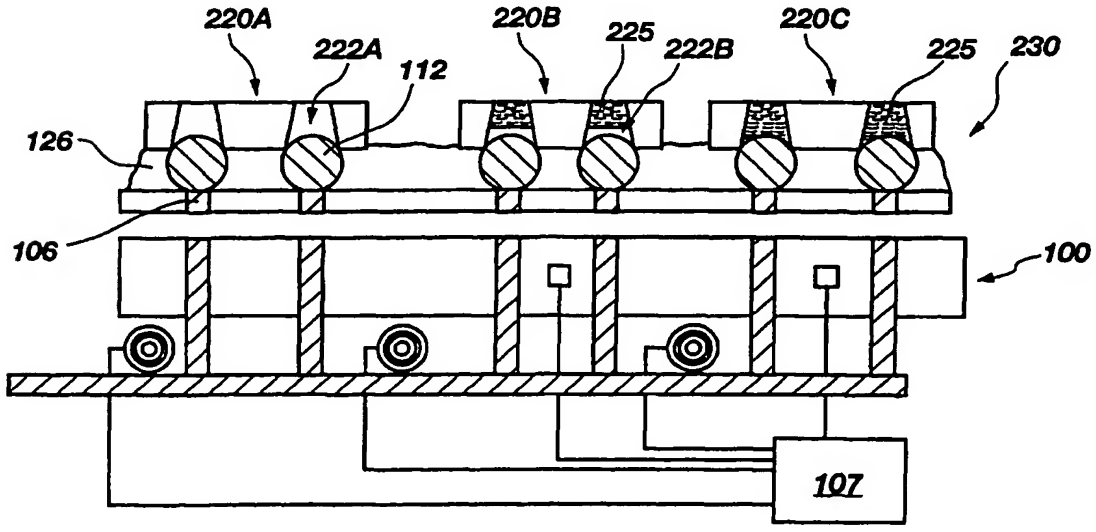

220A
222A
112
220B
225
222B
220C
225
230
126
106
100
107

FIG. 12

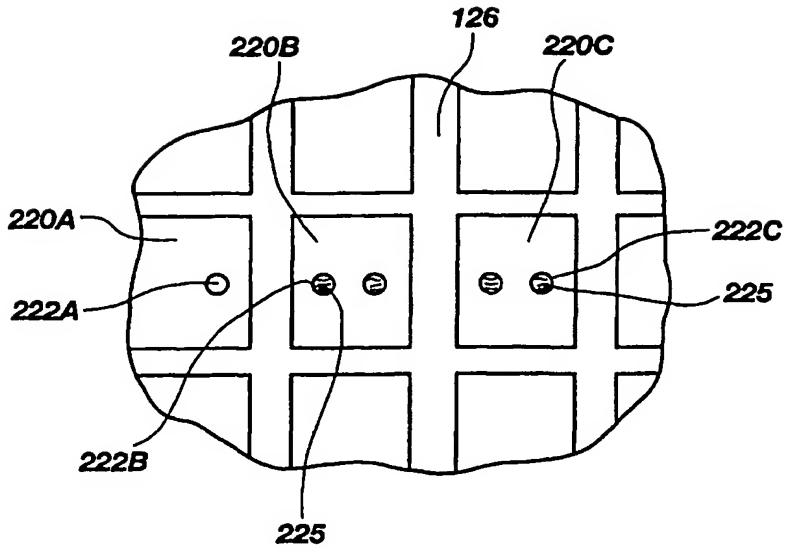


FIG. 12A

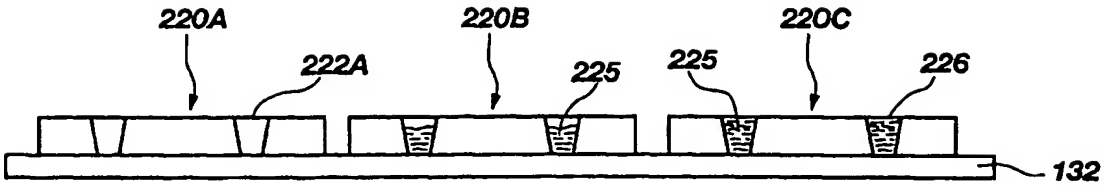
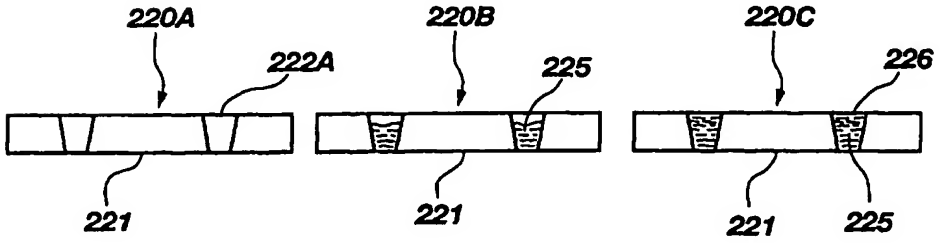

220A
222A
220B
225
225
220C
226
132

FIG. 13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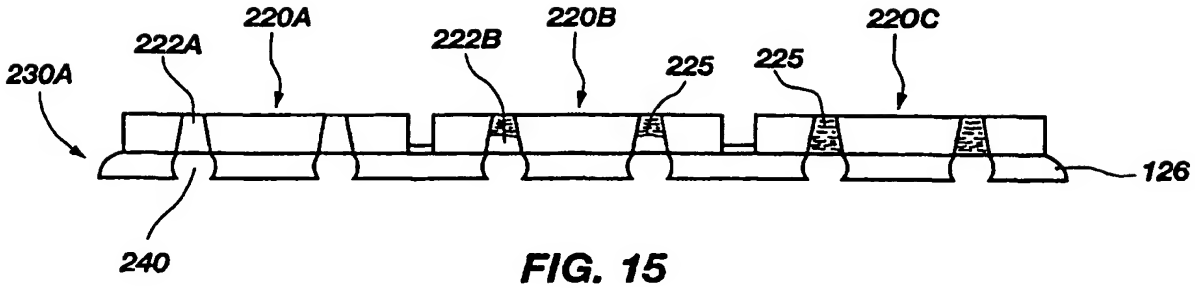
222A
220B
225
220C
226
221
221
221
225

FIG. 14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222A
222B
220B
225
225
220C
230A
126
240

FIG. 15

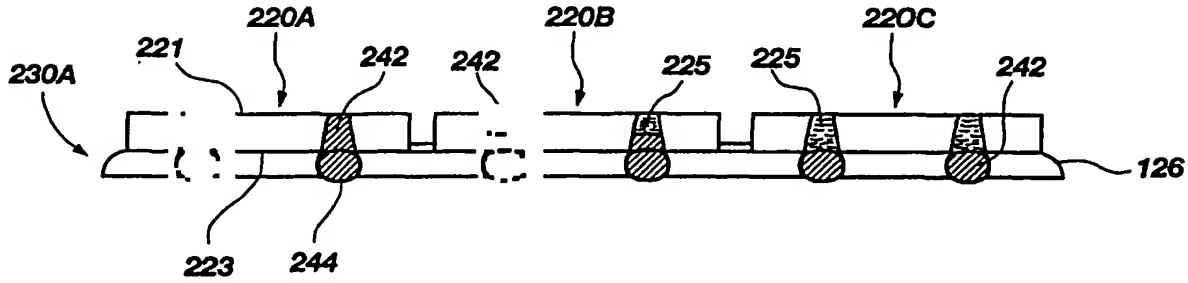
220A
221
242
242
220B
225
225
220C
242
230A
126
223
244

FIG. 16

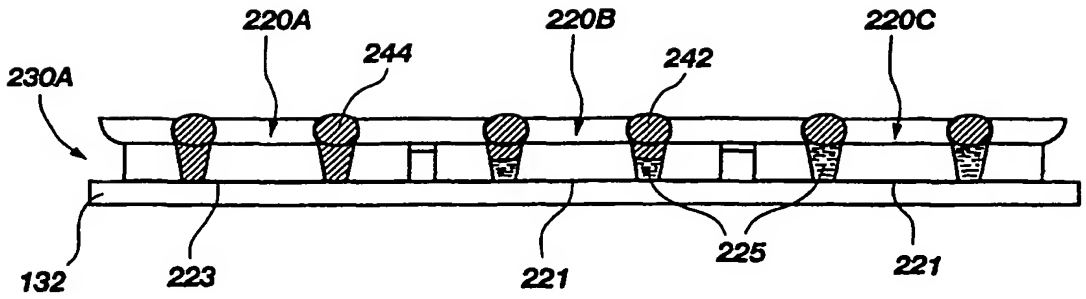
220A
244
220B
242
220C
230A
132
223
221
225
221

FIG. 17

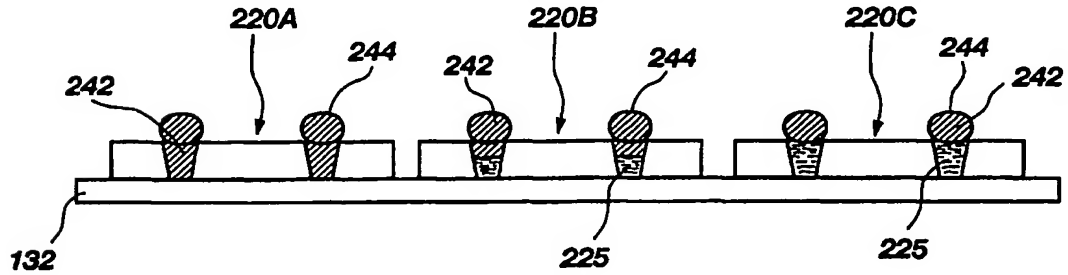
220A
244
220B
242
244
220C
244
242
242
132
225
225

FIG. 18